Electronic Version

Stylesheet Version v1.1.1

# Description

# A Current-Mirrored Crystal-Oscillator Circuit Without Feedback to Reduce Power Consumption

## BACKGROUND OF INVENTION

[0001] This invention relates to crystal-oscillator circuits, and more particularly to oscillator buffers using current-mirror circuits without feedback.

[0002] Electronic systems and devices often must rely on precise clocks to sequence through states, process data, and perform other tasks. Crystal oscillators are often used to generate the precise clocks needed by these systems.

[0003] Figure 1 is a diagram of a prior-art crystal oscillator. Crystal 12 oscillates at a fundamental frequency when a gain stage provides gain to start the crystal oscillating and then to maintain the oscillation. Crystal 12 is coupled between nodes X1 and X2, and is usually connected to other components such as inverter 14 by pins on an integrated circuit (IC). Inverter 14 inverts node X1 and drives node

X2, acting as the gain stage and providing a 180-degree feedback signal to node X2 in relation to node X1. Feedback resistor 10 acts as a DC bias that biases inverter 14 in its gain region.

[0004] Capacitors 16, 18 provide a load capacitance to ground for nodes X1, X2. The value of capacitors 16, 18 can alter the frequency of oscillation of crystal 12. Any given crystal has a manufacturer-specified load capacitance that causes the crystal to oscillate at exactly the specified frequency. Larger capacitive loads on nodes X1, X2 slow down the oscillation, while smaller capacitive loads on nodes X1, X2 accelerate the oscillation.

[0005] The gain of inverter 14 must be large enough to provide a negative resistance to start oscillation. The negative resistance of inverter 14 is cancelled by the positive resistance of crystal 12, since the negative resistance provided by the inverter is equal to the series resistance of crystal. However as the amplitude of oscillations increase, the gain of inverter 14 is reduced by non-linearities of transistors in inverter 14.

[0006] The non-linearity of transistors in inverter 14 can distort the output waveform. Power loss and electro-magnetic interference (EMI) can increase. Higher-amplitude signals

applied to crystal 12 can reduce its long-term stability. The gain of inverter 14 can vary with power-supply voltage Vdd, causing the oscillation frequency to vary with the power supply, which is undesirable.

## Brief Description of Drawings

[0007] Figure 1 is a diagram of a prior-art crystal oscillator.

[0008] Figure 2 is a block diagram of a current-mirrored inverter circuit for a crystal oscillator without feedback.

[0009] Figure 3 is a schematic of a current-mirrored oscillator circuit without internal feedback in the inverter.

## Detailed Description

[0010] The present invention relates to an improvement in crystal-oscillator circuits. The following description is presented to enable one of ordinary skill in the art to make and use the invention as provided in the context of a particular application and its requirements. Various modifications to the preferred embodiment will be apparent to those with skill in the art, and the general principles defined herein may be applied to other embodiments. Therefore, the present invention is not intended to be limited to the particular embodiments shown and described, but is to be accorded the widest scope consistent

with the principles and novel features herein disclosed.

[0011] Figure 2 is a block diagram of a current-mirrored inverter circuit for a crystal oscillator without feedback between stages. Circuit 100 can replace inverter 14 in the crystal oscillator of Fig. 1. The crystal and bias resistor (not shown) are connected between crystal nodes X1 and X2. Circuit-input node 30 is the first crystal node (X1), while circuit-output node 60 is the second crystal node (X2).

[0012] Low-gain input stage 92 receives first crystal node X1 as an input, and buffers node X1 to generate a buffered signal to gain stage 94. Low-gain input stage 92 also inverts the input signal in some embodiments. Low-gain input stage 92 reduces the loading on first crystal node X1, providing a clean signal on the crystal's nodes.

[0013] Gain stage 94 converts the buffered voltage signal from low-gain input stage 92 into a current (V2I conversion) and then provides current gain. Since low-gain input stage 92 buffers first crystal node X1 from gain stage 94, the crystal is not disturbed by the high-gain stage.

[0014] Current mirror 96 mirror the amplified current from gain stage 94 and drives a pull-up and a pull-down driver in output stage 98. High current drive to second crystal node X2 is provided by output stage 98.

[0015] Supply-independent current sources 90 provides current to each of low-gain input stage 92, gain stage 94, current mirror 96, and output stage 98. Noise on the power line is rejected by the supply-independent current sources.

[0016] In contrast to other circuits, no feedback is provided between stages of circuit 100. Instead, signals progressively are generated by subsequent blocks without inter-block feedback signals. Feedback circuits can have a stability problem and can cause noise peaks in the output signal if the damping factor is low.

[0017] Figure 3 is a schematic of a current-mirrored oscillator circuit without internal feedback in the inverter. Capacitor 32 on first crystal node 30 (X1) and capacitor 62 on second crystal node 60 (X2) can be load capacitances or can be adjusted to tune the oscillator frequency. Crystal 44 and bias resistor 42 are coupled in parallel to each other between crystal nodes X1, X2.

[0018] Resistors 28, 42 have a large value, such as 200 K-ohm, and block AC current but allow slower DC bias currents to flow. Since resistors 28, 42 act as AC open circuits, AC currents or small signals on first crystal node X1 only see the gate capacitance of input transistor 34, an n-channel transistor with its source grounded.

[0019] The high resistance of resistor 28 prevents AC signals on first crystal node X1 from passing through to the drain of input transistor 34, and to the gates of transistors 36, 48, which are connected together by buffered node NB. Buffered node NB is driven by source current from current source 22. The drain currents through input transistor 34 and through parallel transistor 36 sink current from buffered node NB. When X1 rises, input transistor 34 increases its drain current, reducing the voltage on buffered node NB, which is also the gate of parallel transistor 36, which then draws less drain current. Thus the total current through transistors 34, 36 remains relatively constant.

[0020] Transistors 34, 36 and current source 22 form the low-gain input stage. Buffered node NB is applied to the gate of converter transistor 48, which converts the voltage on buffered node NB to a current that is limited by source resistor 38 on the source of converter transistor 48.

[0021] The drain current of converter transistor 48 is pulled from amplifier node NA, which received current from current source 24. Current from amplifier node NA is sunk through upper amplifier transistor 46, which is in series with lower amplifier transistor 52. The gate and drain of upper amplifier transistor 46 are connected together at

amplifier node NA and to the gate of upper current mirror transistor 50. The gate of lower amplifier transistor 52 and the gate and drain of lower current mirror transistor 54 are connected together as current-mirror node NC. The current through the channel of upper amplifier transistor 46 is mirrored to the channel current of upper current mirror transistor 50, while the current through lower current mirror transistor 54 is mirrored to lower amplifier transistor 52.

[0022] Current-mirror node NC drives the gate of output transistor 58, which drains current to ground from second crystal node X2, the output node of circuit 100. Pull-up current to second crystal node X2 is provided by current source 26 and p-channel transistor 56 in series. The gate and drain of p-channel transistor 56 are connected together at node X2.

[0023] The drain of upper current mirror transistor 50, drain node ND, is connected to current source 26 and to the source of p-channel transistor 56. Thus the current-mirror and output-stage current is provided by current source 26, while the voltage-to-current and gain stage current is provided by current source 24. Current source 22 provides current to the input stage. Current sources

22, 24, 26 could each be a transistor with a gate driven by a bias voltage. The bias voltage could be generated by a band-gap reference generator or another reference so as to be relatively independent of supply, temperature, and process variations.

[0024] The amplifier current IA through current source 24 can be relatively small to limit voltage swings. Larger AC signals input to first crystal node X1 can result in clipped voltages on second crystal node X2 due to the limited current from current source 24, which limits voltage swings on current-mirror node NC and drain node ND. The large-signal gain is limited to IA/V(X1) when clipping occurs. Larger AC voltages produce reduced gain. Once gain is reduced to the value of the positive resistance of the crystal, the AC input voltage stops increasing.

[0025] Both p-channel transistor 56 and output transistor 58 can operate in the saturated region, resulting in an approximately sine-wave output signal on second crystal node X2. The output impedance of p-channel transistor 56 and output transistor 58 is relatively high, not degrading the Q value of the crystal. Internal nodes can be kept at low impedance to reduce phase shift.

[0026] Operation

[0027] When X1 rises, input transistor 34 increases its drain current, reducing the voltage on buffered node NB, which is also the gate of parallel transistor 36, which then draws less drain current. Thus the total current through transistors 34, 36 remains relatively constant as buffered node NB falls in voltage.

[0028] The lower voltage on buffered node NB is applied to the gate of converter transistor 48, which reduces its drain current. The lower drain current from amplifier node NA shifts more of amplifier current IA through upper amplifier transistor 46 and lower amplifier transistor 52, raising the voltage of amplifier node NA and increasing mirrored current in upper current mirror transistor 50. The higher current through upper current mirror transistor 50 decreases the pull-up current through p-channel transistor 56, helping second crystal node X2 to fall in voltage.

[0029] The larger current through upper current mirror transistor 50 must pass through lower current mirror transistor 54, causing its gate voltage, current-mirror node NC, to rise. The higher voltage on current-mirror node NC is applied to the gate of output transistor 58, increasing the pull-down current from second crystal node X2. Thus the voltage of second crystal node X2 falls when X1 rises. Falling

X1 voltages produces opposite changes, ultimately resulting in X2 rising in voltage. Thus circuit 100 acts as an inverter.

[0030] All substrates of n-channel transistors 34, 36, 46, 48, 50, 52, 54, 58 can be formed in the same P-well or p-substrate and can be tied to ground or to a back-bias voltage below ground. The bulk node of p-channel transistor 56 can be connected to its source, drain node ND.

[0031] ALTERNATE EMBODIMENTS

[0032] Several other embodiments are contemplated by the inventors. For example, capacitors, resistors, and other components may be added, and parasitic components may exist. The standard transistor layout does not have to be used for the capacitors, but other layouts such as doughnut rings or large rectangles with source/drain on 3 sides could be employed. Various improvements in complementary metal-oxide-semiconductor (CMOS) technology and transistors may be employed. Currents, current sources and current sinks can be positive or negative, depending on direction. For example, a negative current source can sink current, such as to ground. Signals, logic, and transistors can be complemented or inverted in a variety of ways. Sources and drains of transistors are often

interchangeable.

[0033] The voltage range of X1, X2, and other nodes could be adjusted or shifted. The crystal nodes X1, X2 could each have both n-channel and p-channel capacitors connected in parallel to adjust oscillator frequency.

[0034] The transistor sources could terminate at a voltage other than ground, or tail resistors could be added. The same is true for the current sources, which could be terminated at a voltage other than the power-supply voltage.

[0035] Any advantages and benefits described may not apply to all embodiments of the invention. When the word "means" is recited in a claim element, Applicant intends for the claim element to fall under 35 USC Sect. 112, paragraph 6. Often a label of one or more words precedes the word "means". The word or words preceding the word "means" is a label intended to ease referencing of claims elements and is not intended to convey a structural limitation. Such means-plus-function claims are intended to cover not only the structures described herein for performing the function and their structural equivalents, but also equivalent structures. For example, although a nail and a screw have different structures, they are equivalent structures since they both perform the function of fastening. Claims

that do not use the word "means" are not intended to fall under 35 USC Sect. 112, paragraph 6. Signals are typically electronic signals, but may be optical signals such as can be carried over a fiber optic line.

[0036] The foregoing description of the embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.